Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended). A process for designing semi-conductor memory components ~~(1), in particular DRAM components, whereby the process comprises the following steps~~ comprising:

- designing of a first layout ~~(2')~~ for a semi-conductor memory module ~~(2)~~ of the semi-conductor memory component ~~(1)~~ to be used for a first configuration of the semi-conductor memory component ~~(1)~~;

- designing of a second layout ~~(2'')~~ for the semi-conductor memory module ~~(2)~~ to be used for a second configuration of the semi-conductor memory component ~~(1)~~, the second layout being different from the first layout;

- using ~~of~~ the first layout ~~(2')~~ or ~~of~~ the second layout ~~(2'')~~ for the total layout of the semi-conductor memory component ~~(1)~~, depending on the particular configuration of the semi-conductor memory component ~~(1)~~, together with at least one further layout for at least one further semi-conductor memory module of the semi-conductor memory component that is identical and not dependent on the particular configuration of the semi-conductor memory component,

wherein the first and second layouts for the semi-conductor memory module have essentially the same external dimensions and are arranged at the same locality of the total layout.

2 (currently amended). A process according to Claim 1, in which the process comprises the following additional steps:

- designing of a third layout ~~(2''')~~ for the semi-conductor memory component module ~~(2)~~ to be used for a third configuration of the semi-conductor memory component ~~(1)~~;

- using of the first, second or third layout ~~(2', 2'', 2''')~~ for the total layout of the semi-conductor memory components ~~(1)~~, depending on the particular configuration of the semi-conductor memory component ~~(1)~~.

3 (currently amended). A process according to Claim 2, ~~in which the first and second, in particular~~ wherein the first, second and third layouts ~~(2', 2'', 2''')~~ for the semi-conductor memory component module ~~(2)~~ all have essentially the same exterior dimensions.

4 (currently amended). A process according to Claim 2, ~~in which the first and second, in particular~~ wherein the first, second and third layouts ~~(2', 2'', 2''')~~ for the semi-conductor memory component module ~~(2)~~ are all essentially arranged at the same locality of the total layout.

5 (currently amended). A process according to Claim 1, in which the process additionally comprises the following steps:

- designing ~~of a~~ the at least one further layout ~~(3)~~ for [[a]] the at least one further semi-conductor memory module ~~(3a)~~ of the semi-conductor memory component ~~(1)~~;

~~using of the further layout (3) for the total layout of the semi-conductor memory component (1), not dependent on the particular configuration of the semi-conductor memory component (1)~~.

6 (currently amended). A process according to Claim 1, in which the semi-conductor memory component ~~(1)~~ is a RAM component.

7 (currently amended). A process according to Claim 6, in which the semi-conductor memory component ~~(1)~~ is a DRAM component.

8 (currently amended). A process according to Claim 7, in which the structure of the DRAM component ~~(1)~~ is essentially identical, as with DRAM components configurable by means of fuses or bonds.

9 (currently amended). A process according to Claim 7, ~~in which the first and second, in particular~~ wherein the first, second and third layouts ~~(2', 2'', 2''')~~, and/or the further layout ~~(3)~~ and/or additional layouts ~~(9', 9'', 9'''; 4', 4'', 4''')~~ - in particular when used jointly – are exclusively suited to be used in semi-conductor memory components ~~(1)~~, in particular RAM or DRAM components.

10 (currently amended). A process according to Claim 1, in which the module ~~(2)~~ is allocated to a relatively high and/or medium semi-conductor component design abstraction level, in particular to a sub-system, algorithm, register transfer, logic and/or module level.

11 (currently amended). A process according to Claim 10, in which the module ~~(2)~~ is not allocated to the highest semi-conductor component design abstraction level, in particular not to the system and/or CPU/memory level.

12 (currently amended). A process according to Claim 1, which produces a total layout for an SDR-DRAM or DDR-DRAM and/or a DDR2-DRAM component, corresponding with the particular semi-conductor memory component configuration selected in each case.

13 (currently amended). A process according to Claim 1, which produces corresponding with the particular semi-conductor memory component configuration selected in each case a total layout for a semi-conductor memory component ~~(1)~~ with a number of data output bits corresponding with the particular configuration.

14 (currently amended). A process according to Claim 1, which produces corresponding with the particular semi-conductor memory component configuration selected in each case a total layout for a semi-conductor memory component ~~(1)~~ with a data and/or clock pulse rate corresponding with the particular configuration.

15 (currently amended). A process according to Claim 1, which produces corresponding with the particular semi-conductor memory component configuration selected in each case a total layout for a semi-conductor memory component ~~(1)~~ with a voltage supply designed in accordance with the particular configuration.

16 (withdrawn). A process for manufacturing semi-conductor memory components (1), in particular DRAM components, whereby the process comprises the following steps:

- designing of a first layout (2') for a module (2) of the semi-conductor memory component (1) to be used in a first configuration of the semi-conductor memory component (1);
- designing of a second layout (2'') for the module (2) of the semi-conductor memory component (1) to be used for a second configuration of the semi-conductor memory component (1);
- using of the first layout (2') or of the second lay-out (2'') for the total layout of the semi-conductor memory component (1), depending on the corresponding configuration of the semi-conductor memory component (1);
- manufacturing of a mask based on the total layout, in particular a photo mask.

17 (withdrawn). A process for manufacturing semi-conductor memory components (1) according to Claim 16, in which the process additionally comprises the step: manufacturing of a semi-conductor memory component (1) by using the manufactured mask, in particular the photo mask.